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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,906	03/28/2001	Keiichiro Wakamiya	50090-290	2402

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/818,906	Applicant(s) WAKAMIYA ET AL.
	Examiner Nitin Parekh	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/20/03 has been entered. An action on the RCE follows.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 and 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (US Pat. 5757078) in view of Brady et al. (US Pat. 5134460).

Regarding claim 1, Matsuda et al. disclose a semiconductor device comprising:

- a semiconductor chip (21 in Fig. 1)
- a plurality of protective insulating layers (23/24/25a-25c) comprising a coating layer (25c in Fig. 1, 4 and 5) covering the surface of the chip, and
- a plurality of connecting conductors and connecting wiring patterns/layers (see conductors in via holes 27 and wiring patterns/layers 29 in Fig. 1) having different diameter/width connected to the surface/electrode of the chip in a staggered arrangement/manner including a connecting conductor (not numerically referenced in Fig. 1; see conductor in the via 27 connecting layer 29 and 31 in Fig. 1) penetrating the coating layer beyond the outside surface of the coating layer

(Fig. 1, 4 and 5; Col. 4, lines 25-55; Col. 4-6).

Matsuda et al. further teach an embodiment (Fig. 4 and 5) where the connecting conductor comprises a plurality of connecting conductors (38/31 and 38'/31), the connecting conductors including the plurality of layers formed of same material such as metals comprising copper and tin/lead solder (38 and 31 respectively in Fig. 3 and 38' and 31 respectively in Fig. 4; Col. 6, lines 36-62; Col. 6, line 11- Col. 7, line 8).

Matsuda et al. fail to teach at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer.

Brady et al. teach using a connecting conductor formed of a plurality of metal layers including titanium, aluminum, titanium/chromium, copper and tin (51-55 respectively in Fig. 3; Col. 7, lines 35-62) where one of the layers being aluminum (52 in Fig. 3) which has lower hardness and is softer than other layer such as copper (Col. 4, line 29; Col. 2, lines 13 and 65). Brady et al. further teach using the soft aluminum metal being beneficial (Col. 4, lines 38-43) to reduce the effects of mechanical stress and excessive force on underlying structures to improve the bonding and to reduce stress related defects (Col. 2, lines 14-16).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one of the conductor layers being formed as a stress absorbing layer having lower hardness than the other layer as taught by Brady et al. so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Matsuda et al's device.

Regarding claim 4, Matsuda et al. and Brady et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Matsuda et al. teach the connecting conductors being formed by stacking a plurality of layers in a staggered

manner (see conductors in the via holes 27 and wiring patterns/layers 29 in Fig. 1; Col. 4, lines 25-55).

Regarding claim 5, Matsuda et al. and Brady et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above, and Matsuda et al. further teach another embodiment having the plurality of layers of the connecting conductors being of substantially identical diameter (31a and 31 in Fig. 8F; Col. 9, line 30).

Regarding claim 6, Matsuda et al. and Brady et al. teach substantially the entire claimed structure as applied to claims 1 and 4 above, wherein Matsuda et al. teach the plurality of layers of the connecting conductors being of different diameter from each other in the sequence of layers (see conductors in via holes 27 in Fig. 1; Col. 4 and 5).

4. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (US Pat. 5757078) and Brady et al. (US Pat. 5134460) as applied to claim 1 above, and further in view of Akagawa (US Pat. 5886415).

Regarding claims 2 and 3, Matsuda et al. and Brady et al. teach substantially the entire claimed structure as applied to claim 1 above, except the connecting conductor being formed from an anisotropic conductive material or a conductive material containing

metal particles respectively.

Akagawa teaches a semiconductor device having connecting conductors connected to a chip surface/electrode (not numerically referenced- see connecting portion above 36/37 in Fig. 2, 3, 7 and 8) where the connecting conductors are formed of an anisotropic conductive material (38 in Fig. 2, 3, 7 and 8; Col. 4, lines 10-25) containing metal particles (39 in Fig. 2, 3, 7 and 8; Col. 1, line 40), the anisotropic conductive material being of low hardness and being functional as a shock absorbing layer to protect the chip/device (Col. 8, lines 1-5; Col. 10, lines 30-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles as taught by Akagawa so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Brady et al. and Matsuda et al's device.

5. Claims 7, 8 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al. (US Pat. 5757078) in view of Brady et al. (US Pat. 5134460) and further in view of Chakravorty (US Pat. 6181569).

Regarding claim 7, Matsuda et al. disclose a semiconductor device comprising-

- a semiconductor chip (21 in Fig. 1)
- a plurality of protective insulating layers (23/24/25a-25c) comprising a coating layer (25c in Fig. 1, 4 and 5) covering the surface of the chip, and
- a plurality of connecting conductors and connecting wiring patterns/layers (see conductors in via holes 27 and wiring patterns/layers 29 in Fig. 1) having different diameters/width connected to the surface/electrode of the chip in a staggered arrangement/manner including a connecting conductor (not numerically referenced in Fig. 1; see conductor in the via 27 connecting layer 29 and 31 in Fig. 1) penetrating the coating layer beyond the outside surface of the coating layer

(Fig. 1, 4 and 5; Col. 4, lines 25-55; Col. 4-6).

Matsuda et al. further teach an embodiment (Fig. 4 and 5) where the connecting conductor comprises a plurality of connecting conductors (38/31 and 38'/31), the connecting conductor; including the plurality of layers formed of same material such as a metal comprising copper and tin/lead solder (38 and 31 respectively in Fig. 3 and 38' and 31 respectively in Fig. 4; Col. 6, lines 36-62; Col. 6, line 11- Col. 7, line 8).

Matsuda et al. fail to teach the plurality of layers of the connecting conductors being

formed of different material and at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer.

Brady et al. teach using a connecting conductor formed of a plurality of metal layers including titanium, aluminum, titanium/chromium, copper and tin (51-55 respectively in Fig. 3; Col. 7, lines 35-62) where one of the layers being aluminum or gold (52 in Fig. 3; Col. '7, lines 40-50), the aluminum having lower hardness and being softer than other layer such as copper (Col. 4, line 29; Col. 2, lines 13 and 65). Brady et al. further teach using the soft aluminum metal being beneficial (Col. 4, lines 38-43) to reduce the effects of mechanical stress and excessive force on underlying structures to improve the bonding and to reduce stress related defects (Col. 2, lines 14-16).

Chakravorty teaches a device having a plurality of the connecting conductors (321 /322 and 321/323/326 in Fig. 10a-10g) connected to a pad on a chip (304 and 302 respectively in Fig. 10a-10g) where one of the plurality of layers (323 and 326 in Fig. 10d and 10g respectively) is formed from a metal/solder material or a conductive polymer material (Col. 14, lines 20-30; Col. 13, line 25- Col. 14, line 35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the plurality of layers of the connecting conductors being formed of different material and at least one of the connecting conductor layers being formed as a stress absorbing layer having lower hardness than the other layer as taught by Chakravorty so that the mechanical stress and chip cracking defects can

be reduced and the desired hardness and bonding strength can be achieved in Brady et al. and Matsuda et al's device.

Regarding claim 8, Matsuda et al. Brady et al. and Chakravorty teach substantially the entire claimed structure as applied to claim 7 above, wherein Brady et al. further teach the stress absorbing layer being formed from gold (52 in Fig. 3; Col. 7, lines 40-50).

Regarding claim 11, Matsuda et al., Brady et al. and Chakravorty teach substantially the entire claimed structure as applied to claim 7 above, wherein Matsuda et al. teach the connecting conductors being formed by stacking a plurality of layers in a staggered manner (see conductors in the via holes 27 and wiring patterns/layers 29 in Fig. 1; Col. 4, lines 25-55).

Regarding claim 12, Matsuda et al., Brady et al. and Chakravorty teach substantially the entire claimed structure as applied to claims 7 and 11 above, and Matsuda et al. further teach another embodiment having the plurality of layers of the connecting conductors being of substantially identical diameter (31 a and 31 in Fig. 8F; Col. 9, line 30).

Regarding claim 13, Matsuda et al., Brady et al. and Chakravorty teach substantially

the entire claimed structure as applied to claims 7 and 11 above, wherein Matsuda et al. teach the plurality of layers of the connecting conductors being of different diameter from each other in the sequence of layers (see conductors in via holes 27 in Fig. 1; Col. 4 and 5).

6. Claims 9 and 10 are rejected under 35 U.S. C. 103(a) as being unpatentable over Matsuda et al. (US Pat. 5757078), Brady et al. (US Pat. 5134460) and Chakravorty (US Pat. 6181569) as applied to claim 7 above, and further in view of Akagawa (US Pat. 5886415).

Regarding claims 9 and 10, Matsuda et al., Brady et al. and Chakravorty teach substantially the entire claimed structure as applied to claim 7 above, except the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles respectively.

Akagawa teaches a semiconductor device having connecting conductors connected to a chip surface/electrode (36 in Fig. 2, 3, 7 and 8) where the connecting conductors are formed of an anisotropic conductive material (38 in Fig. 2, 3, 7 and 8; Col. 4, lines 10-25) containing metal particles (39 in Fig. 2, 3, 7 and 8; Col. 1, line 40), the anisotropic conductive material being of low hardness and being functional as a shock absorbing layer to protect the chip/device (Col. 8, lines 1-5; Col. 10, lines

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the connecting conductor being formed from an anisotropic conductive material or a conductive material containing metal particles as taught by Akagawa so that the mechanical stress and chip cracking defects can be reduced and bonding can be improved in Chakravorty, Brady et al. and Matsuda et al's device.

Response to Arguments

7. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:OOAM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and

703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-3063431.

Nitin Parekh

NP

07-28-03

Nitin Parekh

PATENT EXAMINER

TECHNOLOGY CENTER 2800